

# Optimizing for Eager: Improving Software Transactional Memory through Reservations

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Date and Time: October 19 (Friday), 2012 - 11:00am-12:00pm

Location: 3437 SEC

## **Abstract:**

Concurrency control for multithreaded programs is notoriously difficult for programmers to implement correctly. Transactional memory provides programmers with a clean, high-level interface for specifying required concurrency control, in the form of atomic sections. Unfortunately, it is tricky to implement transactional memory systems and even harder to make them scalable.

In software transactional memory (STM) systems, the compiler and runtime system collaborate to guarantee transactional semantics. I will present a novel extension to the standard compiler/runtime interface, memory reservations, which enables better code generation for so-called eager STM implementations, resulting in less instrumentation and improved speedups on our benchmarks.

This colloquium will be self-contained: I will start by surveying the state of the art on transactional memory, its implementations, and complications, before describing memory reservations.

Memory reservations are joint work with my student, Gaurav Jain.

## **Biography:**

Dr. Patrick Lam is an Assistant Professor of Electrical and Computer Engineering and Associate Director of the Software Engineering programme at the University of Waterloo. He holds a PhD from the Massachusetts Institute of Technology. His research interests are at the intersection of program analysis and software engineering; he can often be found developing analyses for program verification. His non-research interests include scaling mountains and rocks.